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EXPT. NO. 1

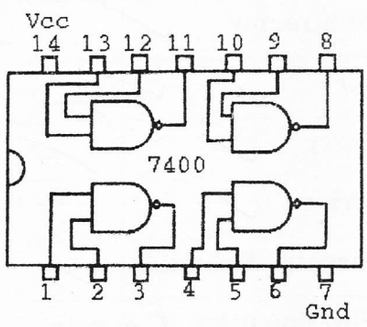
TITLE: **STUDY OF BASIC LOGIC GATES &UNIVERSAL GATES.**

AIM: To study basic gates.

APPARATUS: Power Supply, Breadboard, Connecting wires.

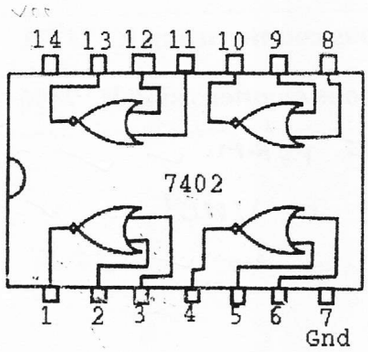
COMPONENTS: ICs 7400, 7402, 7404, 7408, 7432, 7486, LED.

IC PINOUTS

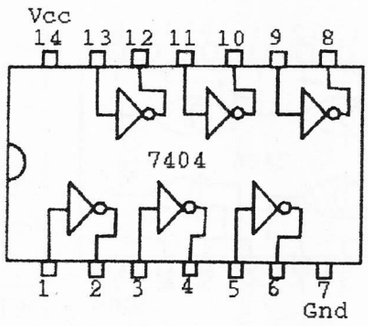


TRUTH-TABLE

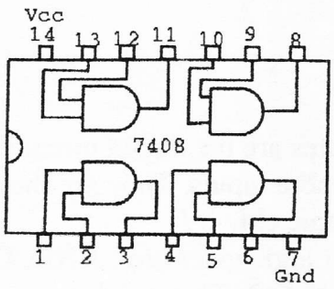
NAND		
A	**B**	**Y=$\overline{A.B}$**
0	0	1
0	1	1
1	0	1
1	1	0



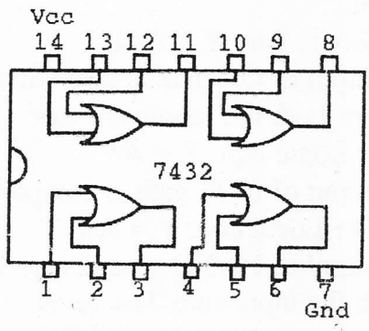
NOR		
A	**B**	**Y=A+B**
0	0	1
0	1	0
1	0	0
1	1	0



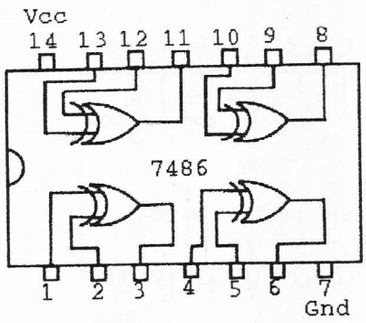
NOT	
A	**Y=A**
0	1
1	0



AND		
A	**B**	**Y=A.B**
0	0	0
0	1	0
1	0	0
1	1	1



OR		
A	**B**	**Y=A+B**
0	0	0
0	1	1
1	0	1
1	1	1



EX-OR		
A	**B**	**Y=AB+AB**
0	0	0
0	1	1
1	0	1
1	1	0

THEORY: Logic gates are the digital circuits with one output and one or more inputs. They are the basic building blocks of any logic ckt.

Different logic gates are : **AND, OR, NOT, NAND, NOR, EX-OR.** They work according to certain logic.

AND : Logic eqn. Y = A.B

The output of AND gate is true when the inputs A and B are True.

OR : Logic eqn. Y = A+B.

The output of OR gate is true when one of the inputs A and B or both the inputs are true.

NOT : Logic eqn. $Y = \bar{A}$.

The output of NOT gate is complement of the input.

NAND : Logic eqn. $\overline{Y = A.B}$

The output of NAND gate is true when one of the inputs or both the inputs are ~~low~~ level.

NOR : Logical eqn. $Y = \overline{A+B}$.

The output of NOR gate is true when both the inputs are low.

EX-OR: Logic eqn. $\overline{Y}=\bar{A}B+A\bar{B}$.

The output of EX-OR gate is true when one and only one input is true.

PROCEDURE: 1)Give biasing to the IC and do necessary connections.
2) Give various combinations of inputs and note down the output with the help of LED for all gate IC,s one by one.
3) Repeat the procedure for all gates.
4) Construct NOT,AND,OR,EX-OR using universal gates & verify it's truth table.

CONCLUSION: Thus all logic gates are studied.

QUESTIONS: 1)What is digital circuit?
2)What is meant by Positive logic and Negative logic?
3)What is Gate?

EXPT. NO. 2

TITLE: **REALIZATION OF LOGICAL EXPRESSION USING BASIC GATES &UNIVERSAL GATES.**

AIM: A)To study realization of basic gates using universal gates.
b)To study realization of logical expression using basic gates & using only Universal gates.

APPARATUS: Power supply,Breadboard,Connecting wires.

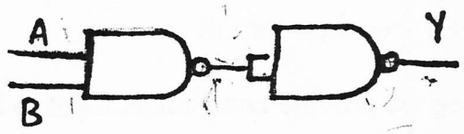
COMPONENTS: ICs 7400, 7402, 7404,7408,7432,7486,LED's

CIRCUIT DIAGRAM:

Using **NAND**

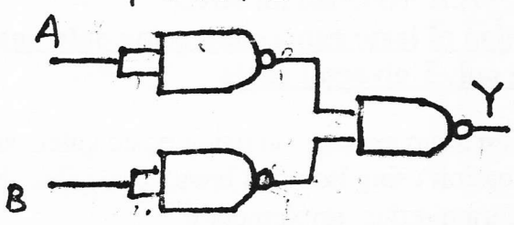
1) AND:-

$Y = A \cdot B$



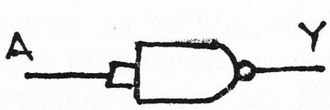
2) OR:-

$Y = A + B$



3) NOT:-

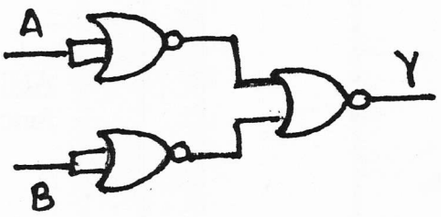
$Y = \overline{A}$



Using **NOR**

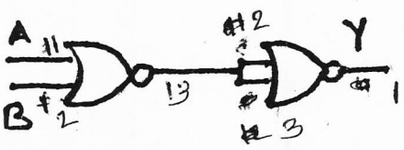
1) AND :-

$Y = A \cdot B$



2) OR:-

$Y = A + B$



3) NOT:-

$Y = \overline{A}$

3)OR = Complimenting the output of NOR gate gives output for OR

OR: Complimenting the output of NOR gate gives output OR

Y=A+B -equation for NOR.
Y=A+B (A=A)
Y=A+B -equation for OR

AND: when we provide complenent input to NOR it function as AND,

Y=A+B -equation for NOR.
=A+B (A+B=A.B)
= A.B (A=A)
=A.B -equation for AND.

Realization of logic expression using only basic gates & using only Universal gates

To realize logic expression using basic gates ,simplify the expression using boolean laws, if possible draw the logic diagram &then implement it.

Realization of logic expression using Universal gates

1)The logic diagram consisting of basic gates can be converted to one having only NAND/only NOR.
2)To convert it to NAND , add bubbles on the output of each AND gate & on input side of all OR gates.
3)To convert it to NOR, add bubbles on the output of each OR gate & on input side of all AND gates.
4)Add or subtract an inverter on each line that received a bubble in step 2 or 3.
5)Replace bubbled OR by NAND & bubbled AND by NOR.
6)Eliminate bubble inversion.
This gives you equivalent NAND/NOR logic diagram.

THEORY:

REALISATION OF BASIC GATES USING UNIVERSAL GATES.

NAND & NOR are called universal gates because using only NAND or only NOR any function can be implemented.

NAND (universal gate):

1)NOT: NAND behaves as NOT when both it's inputs are shorted, to make it single variable.

Y= A.B = equation for NAND gate.

becomes Y= A.A (A.A=A)

Y= A = equation for NOT.

2)AND : Inverting o\p of NAND we get AND gate.

Y= A.B =equation for NAND gate.

Invert it, Y=A.B (A=A)

Y=A.B = equation for AND.

3)OR: If we provided inverted i/p to NAND as an o/p we get OR function.

Y=A.B= equation for NAND gate.

Providing inverted i/p equation becomes

Y=A.B (A.B=A+B)

= A+B

=A+B (A=A)

NOR(Universal gate)

1)NOT :When we short i\p of NOR it behaves as NOT.

Y=A+B -equation for NOR.

Y=A+A -(A+A=A)

Y= A -equation for NOT.

2)AND= when we provide complimented input to NOR it function as AND.

Y=A+$\bar{B}$ -equation for NOR.

=A+B (A+B=A.B)

= A.B (A=A)

= A.B equation for AND.

PROCEDURE:

1) Give biasing to the IC & do necessary connection.
2) Give various combination of i/p's & note down the output.

OBSERVATION TABLE:

A	B	Y
0	0	
0	1	
1	0	
1	1	

CONCLUSION:

Thus realization of basic gates &universal gate is studied.

QUESTIONS:

1)Implement the function using only basic gates &using only universal gates?

1)What is the voltage range for LOW and HIGH level?

2)Implement the function using only basic gates &using only universal gates.Modify the logic equation if necessary by using boolean laws?

Y=~~AC~~ [ABD]+ABCD+ABC

$\bar{A}\bar{C}(ABD') + ABCD + ABC$

$\bar{A} + \bar{C}(ABD')$

$\bar{A} \cdot ABD' + AB\bar{C}D + ABCD + ABC$

$ABC + AB\bar{C}D$

$AB(C + \bar{C}D)$

$ABC + ABD$ 9

$\overline{ABC \cdot ABD}$

$AB(C + D)$

EXPT. NO. 3

TITLE: **ADDER AND SUBTRACTOR**

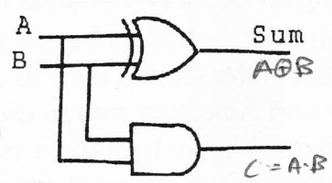
AIM: To study adder and subtractor circuits using logic gates.

APPARATUS: Power supply, breadboard.

COMPONENTS: ICs 7486, 7432, 7408, 7404, LEDs.

CIRCUIT DIAGRAM AND OBSREVATION TABLE :

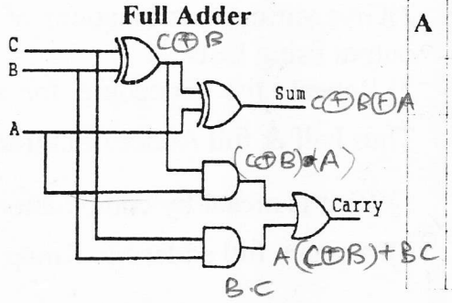
Half Adder



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

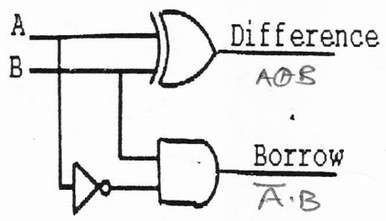
$\bar{A}B + \bar{B}A$

Full Adder



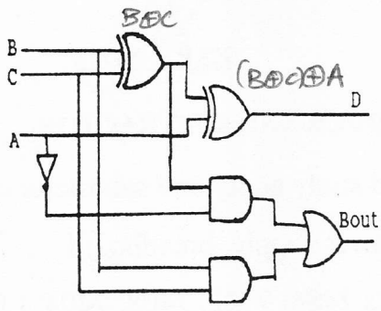
A	B	C	Sum	Carry

Half Subtractor



A	B	Diff.	Bout

Full Subtractor



A	B	C	D	Bout
0	0	0	0	0
0	1	1	0	0
0	0	1	1	1
0	1	0	1	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

THEORY: A digital adder circuit adds binary signals & a subtractor subtracts binary signals. Half Adder/Subtractor is a basic ckt. that adds / subtracts 2 bits and generates sum or difference along with Carry / Borrow. Unlike half adder or subtractor a full adder / subtractor has the provision to take consideration of previous carry / borrow also.

PROCEDURE:
1) Do necessary connections as shown in the ckt. diagram and give biasing to the Ics.
2)Give various combinations of inputs and notedown output using LED.
3) Repeat the procedure for all circuits.

CONCLUSION: Thus half & full Adder / Subtractor is studied.

QUESTIONS:
1)What is meant by combinational circuit?
2)Design a full adder by Kmap method.

A	B	C	Di	Bo
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

EXPT. NO . 4

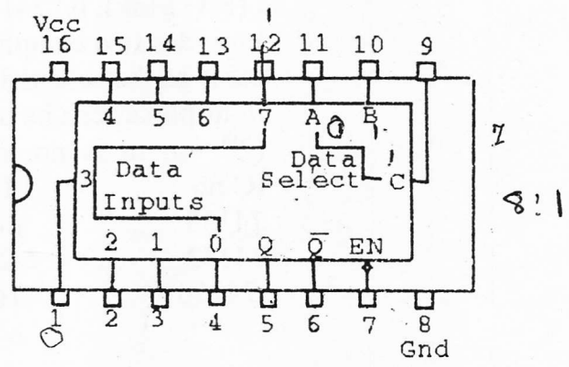
TITLE **MULTIPLEXER**

AIM 1)To study4:1,8:1,16:1 multiplexer.
2)Design & implement 4:1 multiplexer using NAND &NOR gates.

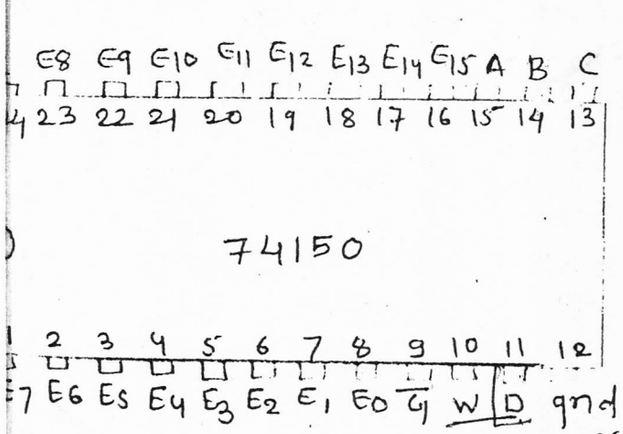
APPARATUS Power supply, Breadboard,connecting wires.

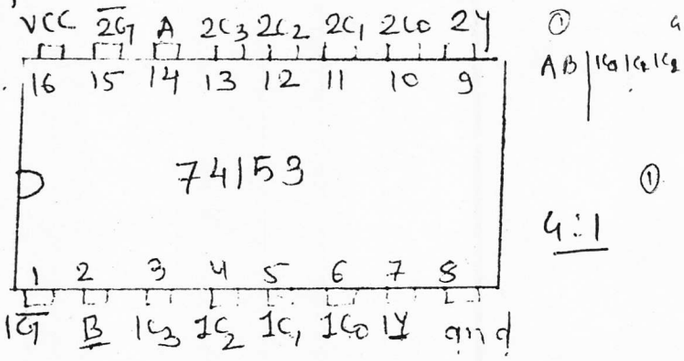
COMPONENTS IC 74151, 74150,74153,.7400,LEDs.

IC PINOUT



IC 74151





THEORY:

Multiplexer is a combinational ckt. that is one of the most widely used in digital design. The multiplexer is a data selector which gates one out of several i/ps to a single o/p. It has n data i/ps & one o/p line & m select lines where $2^m = n$. Depending upon the digital code applied at the select inputs one out of n data input is selected & transmitted to a single o/p channel. Normally strobe(G) input is incorporated which is generally active low which enables the multiplexer when it is LOW. Strobe i/p helps in cascading. A 4:1 Mux. using NAND gate can be designed as shown in dgm 1. No. of ICs are available such as 74157, 74158 (Quad 2:1 mux), 74352, 74153 (dual 4:1 Mux.), 74151A, 74152 (8:1 Mux.), 74150 (16:1 Mux). IC 74151A is a 8 : 1 multiplexer which provides two complementary o/ps Y & Y. The o/p Y is same as the selected i/p & Y is its complement. The n:1 multiplexer can be used to realize a m variable function. ($2^m = n$, m is no. of select inputs)

IC no	Description	output
74153	dual 4:1 mux	same as input
74152	8:1 mux	inverted input
74150	16:1 mux	inverted inputs

A)To pmplement certain function using mux. for eg. F(A,B,C,D) =∑m(0,2,3,6,8,9, 12,14).since there are four variables,a mux with four select input is required.so,16:1 mux is required. connect the i/p lines 0.2.3.6.8.9, 12,14 to logic 1 &others to logic 0.if the o/p of mux is active high. If o/p is active low interchange 1 with 0.

B)Design &implement 4:1 mux using NAND

Truth table of a 4:1 mux

select inputs		outputs
S1	S0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

With low i/p at G, the o/p Y can be expressed as

$Y = S_1S_0I_0 + S_1S_0I_1 + S_1S_0I_2 + S_1S_0I_3$

PROCEDURE:

CASE A)

1)Study 4:1,8:1,16:1 using IC 74153,74150,74152 respectively.

2)Implement the function

F(A,B,C,D) =Σm(0,2,3,6,8.9,12,14) using IC 74150&74152

3)Do the necessary connection & observe the output for different input combination

CASE B)

1)Implement the 4:1 mux using strobe input &IC 7400

2) Do the necessary connection & observe the output For different input combination

CONCLUSION:

1)4:1,8:1,16:1 are studied.

2)4:1 mux using Nand gate is implemented

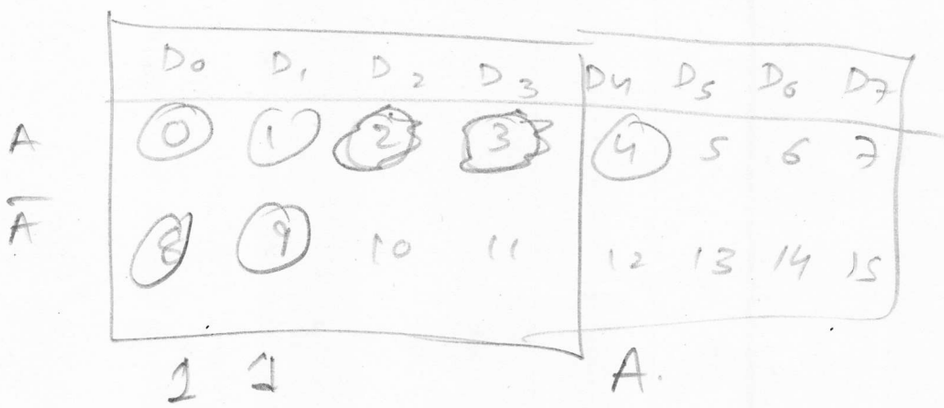
QUESTIONS:

1)Design 4:1 mux using NOR gate.

2) Connect two 74150 ICs & Verify it"s operation as 32:1 Mux

1) Implement 32:1 mux using 2 16:1, & 2:1 MUX

2) Implement $F(A,B,C,D) = \Sigma m(0,1,4,8,9)$ using 8:1 MUX



EXPT. NO. 5

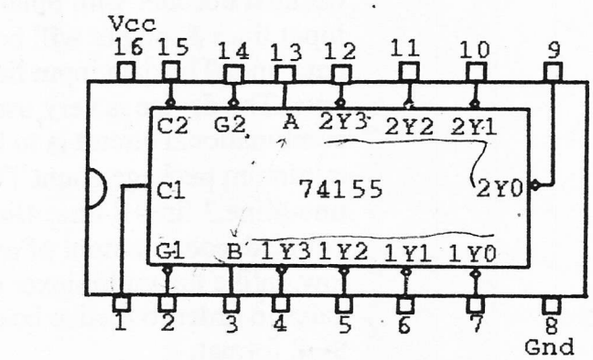
TITLE: **DEMULTIPLEXER**

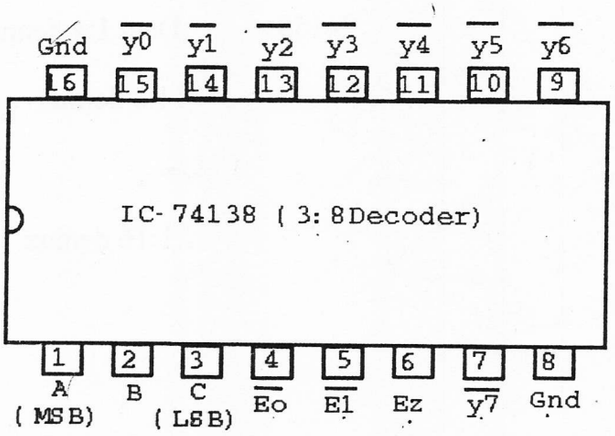
AIM: To study 1:4,1:8,1:16 demultiplexer.

APPARATUS: Power supply, Breadboard,connecting wires.

COMPONENTS: IC 74155, 74138,74154,LEDs.

IC PINOUT:





THEORY:

Demux takes single i/p & distributes it over several o/ps. It accepts a single input & distributes it over several outputs. The select input code determines to which output the data input will be transmitted.

The no. of output lines is n & the no. of select lines is m, where $n=2^M$. This circuit can also be used as Binary to decimal decoder with binary input applied at the select input lines & output will be obtained at the corresponding data lines.The data input line is to connected to logic 1 level.The device is very useful in multiple output combinational circuit is to be designed because this needs minimum package count.These devices are available as 2 line-4line,3 line- 8 line, 4line
16line decoder. output of most of these devices are active low.unlike the multiplexer decoder doesn't require some gates in order to realize boolean expression in standara SOP format.

IC No.	Description	Output
74155	Dual 1:4 demux	1Y-inverted input 2Y-same as input
	1:8 demux	Inverted input
	1:16 demux	same as input

PROCEDURE:

1)Give biasing to the IC.
2)Do necessary connections.
3)Verify the operation of 1:4,1:8,1:16 Demux usine IC.
4) Implement 5 line to 32 line decoder using suitable decoder logic.

OBSERVATION TABLE:

Inputs				Outputs			
Select		Strobe	Data	$1Y_0$ $2Y_0$	$1Y_1$ $2Y_1$	$1Y_2$ $2Y_2$	$1Y_3$ $2Y_3$
B	A	G_1/G_2	C1/C2				

2-Line to 4-Line Decoder OR 1-Line to 4-Line Demultiplexer

INPUTS						*OUTPUTS*							
E1	E2	E3	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7

3:8 decoder

CONCLUSION: Thus demux.it's cascading & to implement multiple output function combinational logic design is studied

QUESTION:

1)Implement the following multiple output function using demux

$F1(A,B,C) = \sum m(0,1,3,7)+d(2,5)$

$F2(A,B,C) = \sum m(1,5,7)$

$F3(A,B,C) = \sum m(0,2,4,6)$

2) Design & implement full adder using suitable decoder logic.

EXPT. NO. 6

TITLE: **DECODER/ DRIVER FOR DISPLAY DEVICE**

AIM: To study BCD to 7-segment decoder/driver using IC7447.

APPARATUS: Power supply, Breadboard,connecting wires.

COMPONENTS: ICs 7447,display device.

THEORY: In many digital system we prefer to see the output in decimal format.Seven segment display is the most popular display device used in digital systems.For displaying data using this device ,the data have to be converted from BCD to 7-segment code.A no. of MSI IC's are available for performing this function.the decoder /driver has 4 input lines for BCD data &7 output lines to drive 7 segment display.output terminals a through 9 of the decoder are to be connected to a through 9 terminals of the display respectively. If the outputs are active low,then the 7-segment LED must -are active low,then the 7 segment LED must be of common anode type,whereas if the output are active high then the 7 segment LED must be of common cathode type.available BCD-7 segment decoder IC's are given in a table.

IC NO	*OUTPUT*	*RATING*	*FACILITIES AVAILABLE*			
			LT	RBI	RBO	BI
7446,74246	Active low,open collector	30V,40MA	YES	YES	YES	YES
7447,74247	Active low,open collector	15V,40MA	YES	YES	YES	YES
7448,74248	Active high,pull up resistor 2K.ohm	5.5V,6.4ma	YES	YES	YES	YES
7449,74249	Active high,open collector	5.5V,8MA	NO	NO	NO	YES

LT(Lamp test):

This is used to check the segment of LED.If it is connected to logic 0 level ,all the segments of the display connected to the decoder will be ON.For normal decoding operation ,this terminal is connected to logic 1 level.

RBI (Ripple blanking input):

It is connected to logic 1 for normal decoding operation.If it is connected to 0 level, the segments output will generate data for normal 7 segment decoding for all BCD input except 0.Whenever the BCD input corresponds to 0, the 7 segment display switches off.This is used to blanking out leading zero's in multidigit display.

RBO (Ripple blanking output):

This output which is normally at logic 1 level goes to logic 0 during zero blanking interval.This is used for cascading purposes & is connected to RBI of the succeding stage.

BI(Blanking input):

If it is connected to logic 0 level,display is switched off,irrespective of BCD inputs. this is used for conserving power in multiplexed displays.

CIRCUIT DIAGRAM:

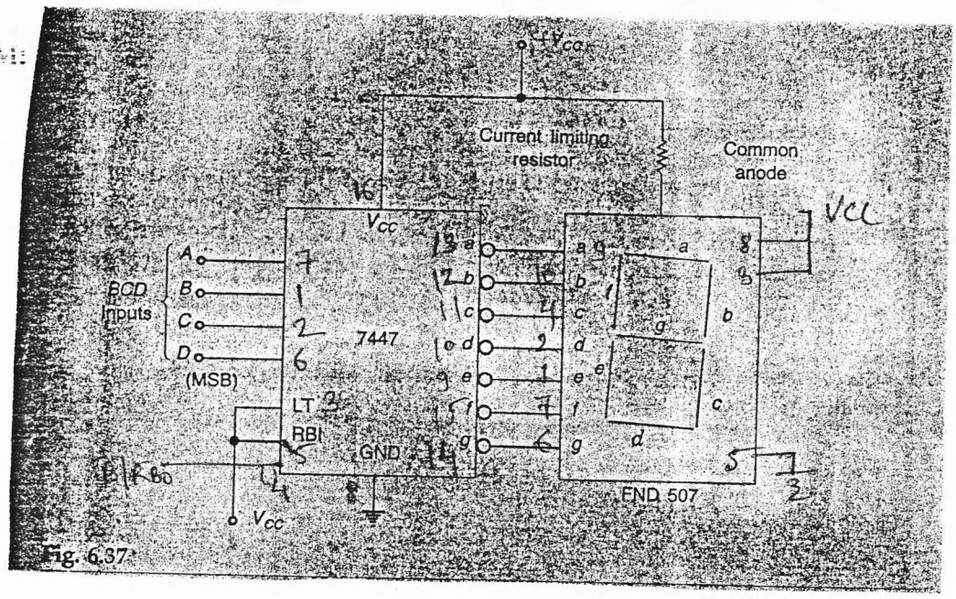


Fig. 6.37

A 7447 driving a 7-segment LED display.

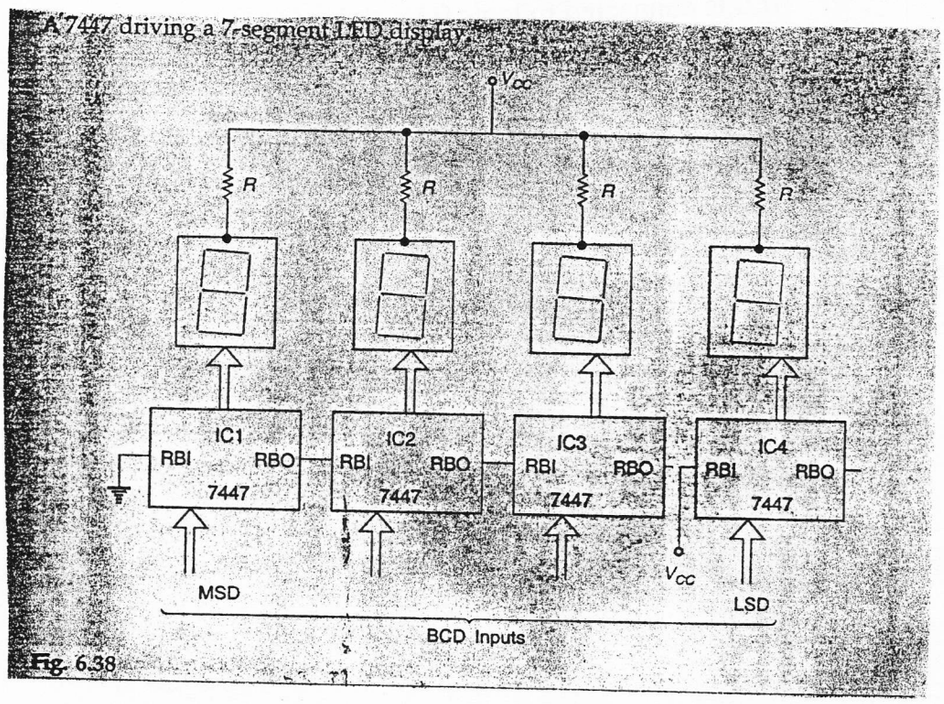


Fig. 6.38

4 digit LED display system with leading zero blanking

PROCEDURE: 1)Do necessary connection.
2)Observe the output by providing different input combinations.

CONCLUSION: BCD to 7-segment decoder is studied.

Question:

7

TITLE **PARITY GENERATOR AND CHECKER**

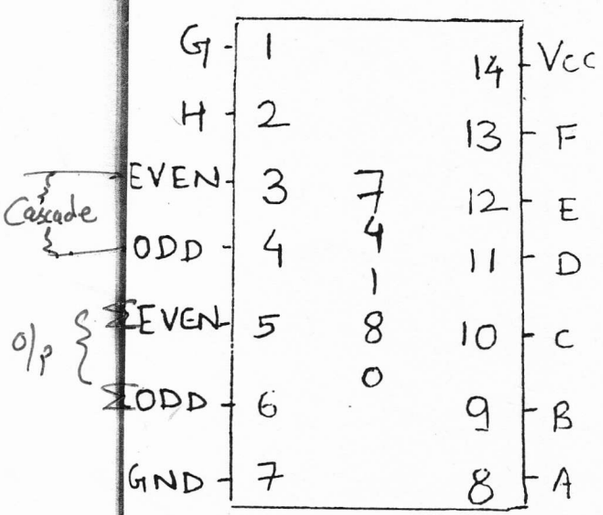
AIM Study of parity generator and checker using IC 74180

1. Verify the function table.
2. Design ~~10~~ 8,9 bit even parity generator.
3. Design ~~10~~ 9 bit even parity checker.

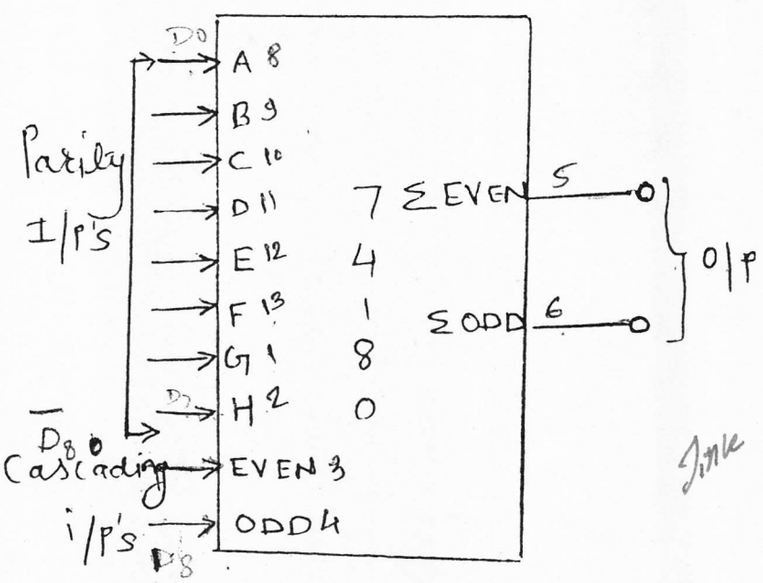
APPARATUS Power supply, breadboard, connecting wires

COMPONENTS IC 74180, LED's

PINOUT DIAGRAM



BLOCK DIAGRAM



0000 0110 → 0
∴ → 1

10100011

3 → E → 1
4 → O → 0

25

THEORY

1) A parity bit is used for the purpose of detecting errors during transmission of binary information.

2) It is an extra bit included with the binary message to make no of 1's Odd or Even. This message is then transmitted and then checked at the receiving end for errors.

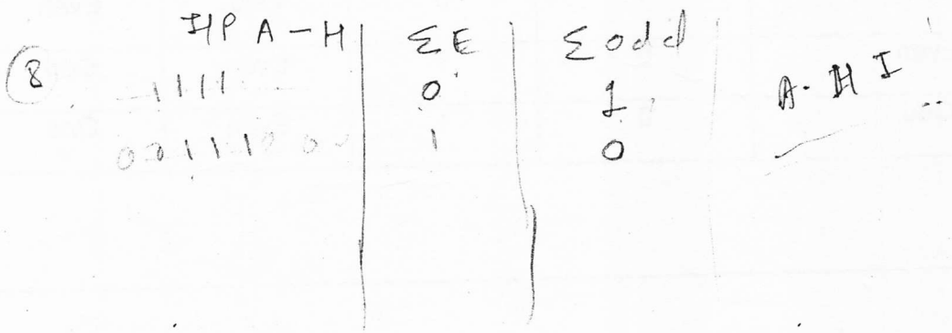
3) An error is detected if the transmitted parity doesn't match with the received one.

4) The circuit that generates the parity bit at the transmitter is called Parity Generator and the circuit that checks the parity at the receiver is called Parity Checker.

5) IC 74180 can work as Parity Generator as well as Parity Checker

PROCEDURE

1. Do necessary connection for the IC to work as 8 bit parity checker
2. Give various 8 bit parity i/p. cascading i/p must not be Equal note down o/ps.
3. Do necessary connection for the IC to work as 9 bit parity Generator
4. Give various 8 bit parity i/p. Note down o/p's.



FUNCTION TABLE AS A 8 BIT PARITY CHECKER

Parity of i/p's A through H	Cascading i/p's		output	
	Even	Odd	∑Even	∑Odd
Even	1	0	1	0
Odd	1	0	0	1
Even	0	1	0	1
Odd	0	1	1	0
×	1	1	0	0
×	0	0	1	1

FUNCTION TABLE AS A 9 BIT PARITY GENERATOR

Parity of i/p's A through H	Cascading i/p's		Parity of i/ps A through H and ∑Even	Parity of i/ps A through H and ∑Odd
	Even	Odd		
Even	1	0	Odd	Even
Odd	1	0	Odd	Even
Even	0	1	Even	Odd
Odd	0	1	Even	Odd

QUESTIONS 1) Design a 10 bit Even Parity Generator using single IC 74180 and an Inverter. Verify its operation.

2) Design a 10 bit Even Parity Checker.

EXPT. NO.8

TITLE: **STUDY OF FLIP-FLOPS USING IC &GATE.**

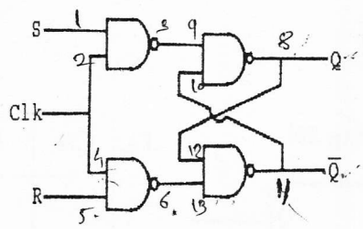
AIM: To study R-S, J-K, D and T flip-flops using IC 7476.

APPARATUS: Breadboard, Power supply.

COMPONENTS: ICs 7400, 7402, 7476, LED.

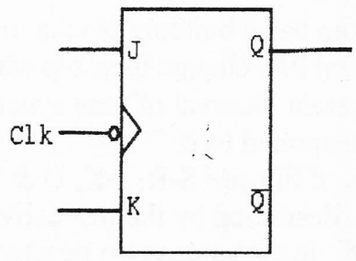
CIRCUIT DIAGRAM AND TRUTHTABLE:

I) SR FF using NAND

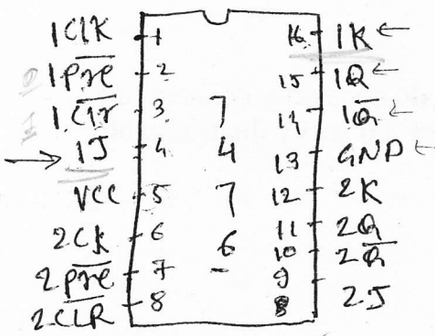


Clk	S	R	Qn
0	X	X	
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	Toggle

II) JK FF (IC 7476)

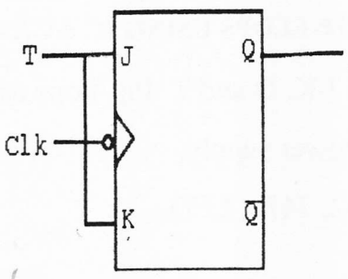


Clk	J	K	Qn
	0	0	Qn
	0	1	0
	1	0	1
	1	1	$\bar{Q}n$



PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⊓	0	0	Qn	$\bar{Q}$n
H	H	⊓	0	1	0	1
H	H	⊓	1	0	1	0
H	H	⊓	1	1	$\bar{Q}$n	Qn

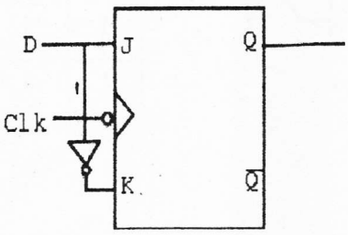
III) T FF using JK



Clk	T	Qn
	0	1
	1	0

Padman Smruti,
Yamuna Baug,
Dewade, T.P. Vasai,
Dist. Thane - 401201

IV) D FF using JK



Clk	D	Qn
	0	0
	1	1

J 4 → 1
K 16 → 2

THEORY: Flip-flops are the basic building blocks of sequential ckt. The clocked FFs change their o/p state depending upon i/p's at certain interval of time synchronized with the clock pulse applied to it.
Different types of FFs are S-R, J-K, D & T . Their operations are described by the respective truthtables.
MSI chip 7476 incorporates two negative edge triggered Master–Slave JK flipflops. The J-K flipflop can be converted to D & T flipflop.

PROCEDURE: 1)Give biasing to the IC and do necessary connections.
2)For various combinations of i/p verify the truthtable.

CONCLUSION: Thus R-S, J-K, D & T Flip-Flops are studied.

QUESTIONS:
1)Construct clocked S-R FF using only NAND gates & verify the truthtable.
2)Verify the truthtable of J-K FF using IC 7476. Observe the effect of Preset & Clear i/ps.
3)Convert the J-K FF to D & T FF.

EXPT NO: 9

TITLE **UNIVERSAL SHIFT REGISTER**

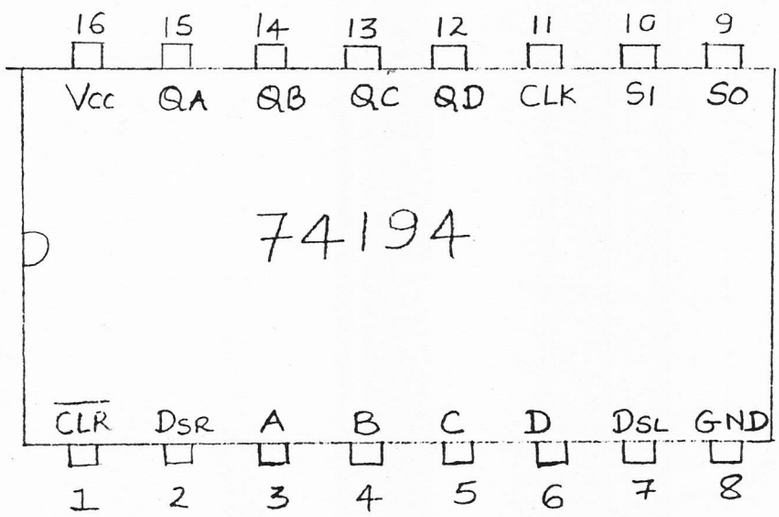
AIM

1. To study different modes of operation of Universal Shift Register using IC 74194
2. Implement Ring counter and Johnson counter using the same IC.

APPARATUS D.C Power supply (5v), function generator, bread board, connecting wires, etc.

COMPONENTS IC 74194, LED's resistor (180 ohm, ¼ watt), etc.

PINOUT DIAGRAM



THEORY

IC 74194 is an MSI 4 bit bidirectional parallel in parallel out shift register. Its contents may be shifted in either of two directions. Left (QD to QA) or right (QA to QD) depending on control input applied.

FUNCTION TABLE

Function	Inputs		Next State				Clear
	S1	S0	QA	QB	QC	QD	
Hold	0	0	QA	QB	QC	QD	1
Shift Right	0	1	Rin	QA	QB	QC	1
Shift Left	1	0	QB	QC	QD	Lin	1
Load	1	1	A	B	C	D	1
Clear	X	X	0	0	0	0	0

PROCEDURE

1. Connect the 5v supply to the IC
2. Apply clock signal of suitable frequency.
3 Observe the operation of the shift register in SIPO (shift right, shift left) PIPO modes

OBSERVATIONS

Sr. No.	Controlling i/p			Data Inputs						Present State				Next State			
	clr	S1	S0	Lin	Rin	A	B	C	D	QA	QB	QC	QD	QA	QB	QC	QD
1	1	0	0														
2	1	0	0														
3	1	0	0														
4	1	0	0														
5	1	0	1														
6	1	0	1														
7	1	0	1														
8	1	0	1														
9	1	1	0														
10	1	1	0														
11	1	1	0														
12	1	1	0														
13	1	1	1														
14	1	1	1														
15	1	1	1														
16	1	1	1														

QUESTION Design a self correcting Ring counter and Johnson counter using the same.

EXPT NO: 11

TITLE **SYNCHRONOUS COUNTER**

AIM Study of Synchronous counter using IC 74191

APPARATUS Power supply, breadboard, Function generator

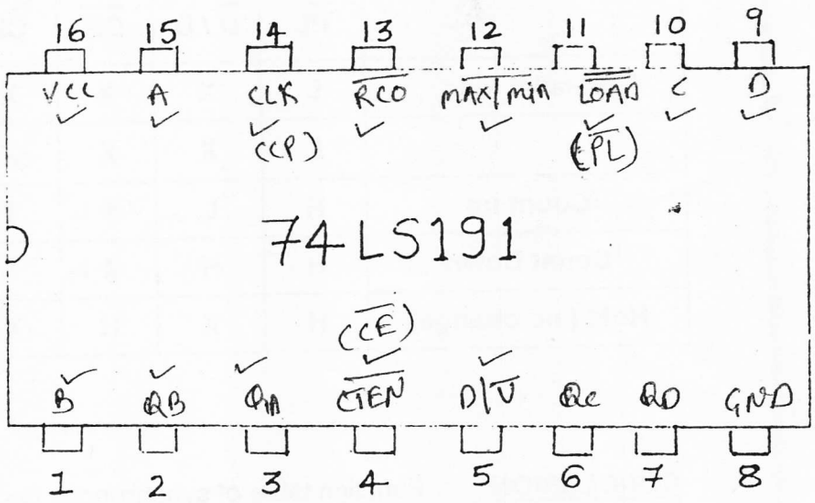
COMPONENTS IC 74191, LED's

PINOUT DIAGRAM

A B C D

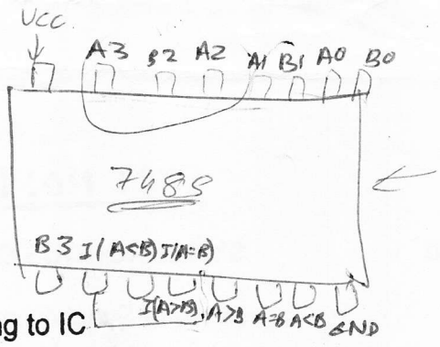
MSB LSB

Q_D Q_C Q_B Q_A



THEORY

IC 74191 is a synchronous up / down counter. It is a 4 bit binary counter. It contains 4 master slave Flip Flops with internal gating and steering logic to provide asynchronous preset ant synchronous count up, count down operations. Its asynchronous parallel load capability permits the counter to be preset to any number. The information present on parallel data inputs (A, B, C, D) is loaded into the counter and appears on the output when $\overline{PL}$ is active low. This operation has got highest priority over the counting operation. The counting is enabled when $\overline{CE}$ is active low. The clock signal is a low to high transition valid signal. $\overline{UP}$ / DOWN determines up counting and down counting.



PROCEDURE

1. Give biasing to IC
2. Verify its function table

FUNCTION TABLE

Operating Mode	Inputs					Outputs
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_N Q_B Q_C Q_D
Parallel load	L	X	X	X	L	L A B C D
	L	X	X	X	H	H X
Count up	H	L	L	↑	X	Count up +1
Count Down	H	H	L	↑	X	Count Down −1
Hold (no change)	H	X	H	X	X	no change

CONCLUSION Function table of synchronous counter was verified.

ASSIGNMENT ABCD = 0000

operating mode	Inputs						o/Ps
	LOAD	CLK	CTEN	U/D	MAX/min	RCO	Q_D Q_C Q_B Q_A
~~Parallel load~~	L	X	X	X	X	X	0 0 0 0
count up	1	⎍	0	0	0	0	0 0 0 0
	⋮	⋮	⋮	⋮	⋮	⋮	1 1 1 1
count Down	1	⎍	0	1	0	0	1 1 1 1
	1	⎍	0	1	0	0	1 1 1 0
	⋮	⋮	⋮	⋮	⋮	⋮	0 0 0 0
Hold (NO change)	1	X	1	X	0	0	no change

EXPT NO: 10

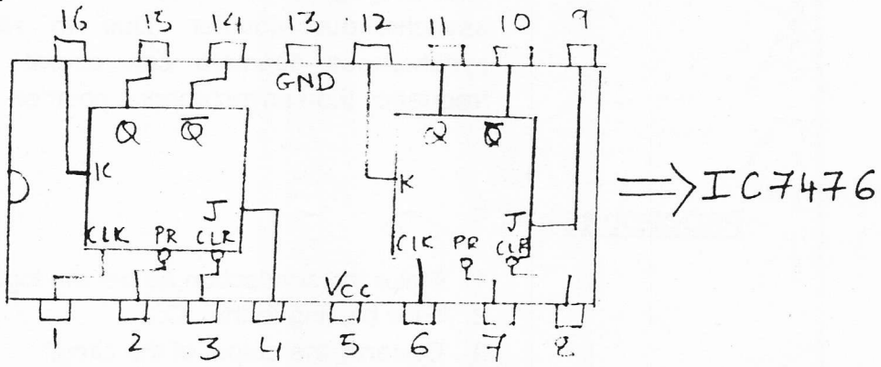
TITLE **SYNCHRONOUS COUNTER**

AIM To design and implement Synchronous counter using IC 7476.

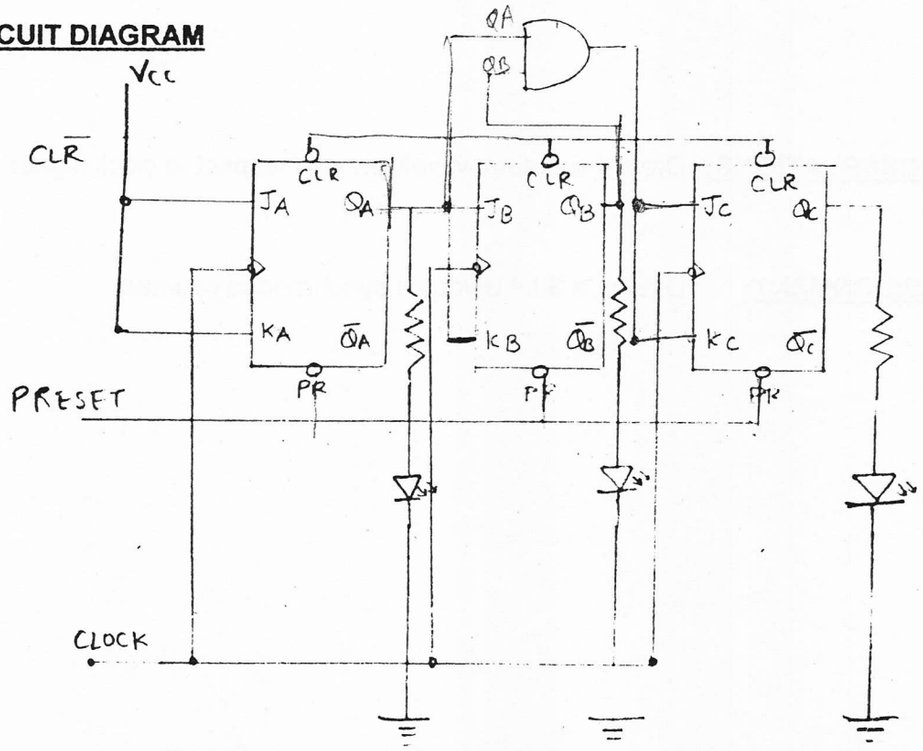
APPARATUS Power supply , breadboard, function generator, connecting wires.

COMPONENTS IC 7476, LED's, IC 7404

PINOUT DIAGRAM



CIRCUIT DIAGRAM



THEORY

In this counter all flip flops are synchronized with the common clock. These counters are faster than asynchronous counters. Since all the flip flop's are clocked at the same time, propagation delay is reduced to a greater extent. Total propagation delay between instant at which the MSB output changes is equal to the sum of propagation delay of one flip flop and that of one AND gate .

Total Propagation Delay= td of one Flip Flop + td of one gate.

This propagation delay is much lesser than the delay present in asynchronous counter. Due to reduced propagation delay, synchronous counters can operate at a much higher clock frequency than asynchronous counters.

PROCEDURE

1. Make the connection as per the logic Diagram.
2. Give biasing to the IC.
3. Observe the output of the circuit.

OBSERVATIONS: Draw the output waveform with respect to clock signal.

ASSIGNMENT: Design a 3 bit up/down synchronous counter.